IJAREEIE

e-ISSN: 2278-8875
p-ISSN: 2320-3765

International Journal of Advanced Research

in Electrical, Electronics and Instrumentation Engineering

Volume 10, Issue 4, April 2021

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.122

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004014

An Energy Efficient of Shift Register Based on Decoder Enabled Gated Pulsed Latch

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ABSTRACT: A VLSI circuit fundamental building block is a change log. Many systems utilize shift registers, like optical filters, contact receivers, and image processing ICs. The word duration of the shifter register has recently increased to process massive picture data in image processing ICs, as the scale of image data continues to grow due to the high demand for high quality image data. To build a low-power and area-efficient shift register, the proposed work employs a decoder-enabled pulsed latch. By replacing flip-flops with pulsed latches, you can save space and electricity. Instead of using a single pulsed clock signal, this approach addresses the timing issue between pulsed latches by using several non-overlap delayed pulsed clock signals. By sorting the latches into multiple sub shifter registers and utilizing extra temporary storage latches, the change register only uses a limited amount of the pulsed clock signals. Using a Xilinx FPGA, a 16-bit shift register with pulsed latches was developed. As opposed to a traditional shift register with flip-flops, the proposed shift register saves both space and strength.

KEYWORDS:- Latch, Shift Register, Decoder, Flip-flop and Clock

I. INTRODUCTION

Energy-saving techniques have become increasingly important in hardware design in recent years, especially for mobile devices. This paper examines many prior prototypes of double edge-triggered flip-flops and proposes a clock-gating double edge-triggered flip-flop centered on transmission gates. As opposed to previous work on double edge-triggered flip-flops, the new one saved 33.14 percent power on average (switching operation factor = 0-0.4), and it can save up to 97.85 percent power while the input is idle as compared to conventional single edge-triggered flip-flops. Furthermore, the proposed architecture increased efficiency by 0.21 ns in Clk-to-Q latency. This paper introduces novel methods for evaluating the energy and latency of flip-flop and latch prototypes, demonstrating that no particular design performs well over the vast spectrum of operating regimes encountered in complex systems. We consider using a variety of flip-flop and latch styles, each optimized for various activation patterns and speeds. On a pipelined MIPS processor datapath running SPECint95 benchmarks, we demonstrate our methodology by reducing overall flip-flop and latch energy by over 60% without raising cycle time. We suggest a series of guidelines for estimating the actual output and power features of flip-flop and master–slave latch systems consistently in this paper. The authors propose a modern simulation and optimization method that addresses both high efficiency and power budget concerns. In various architecture models, the research methodology shows the origins of output and power-consumption bottlenecks. Certain deceptive criteria have been appropriately adjusted and weighted to represent the true properties of the systems under consideration. Furthermore, the contrast of representative master–slave latches and flip-flops demonstrates the benefits of our method as well as the suitability of various product models for high-performance and low-power applications. The standard D flip-flop uses a lot of fuel. So, in this article, we list a new low-power dual-edge triggered Flip-Flop (DETFF) architecture built in 90nm CMOS technology [1]-[5]. As opposed to static output-controlled discharge Flip–Flop, DETFF will accomplish the same data density with half the clock frequency (SCDFF). An explicit pulse generator and a lock that absorbs the pulse signal are used in SCDFF. SCDFF has two static phases of its latch configuration. The pre charge transistor is driven by input D in the first step, causing node to obey D throughout the sampling time. The traditional and proposed DETFFs are introduced and compared in this paper under the same simulation conditions. As a result, the DETFF architecture proposed here is well suited to low-power and small-area applications. Furthermore, non-ideal clock propagation causes clock degradation as well as power supply noise and

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crosstalk. The clocking network and the Flip-Flops dissipate between 30 percent to 70 percent of the overall power in the device.

The use of storage elements capable of recording data on both growing and dropping edges is an alternate clocking method. Dual-Edge Triggered Flip-Flops are a type of storage feature (DETFFs). As opposed to single edge induced Flip-Flops, the same data output can be obtained at half the clock frequency. Double edge clocking may also be used to conserve half of the electricity consumed by the clock delivery network [6]-[10]. The conditional precharge and conditional capture technologies are studied and graded in this paper as high-performance flip-flops. This grouping is dependent around how redundant internal swapping operations may be avoided or reduced. The conditional discharge flip-flop is a new kind of flip-flop (CDFF). It is focused on conditional discharge technology, which is a modern technology. Although retaining the negative initialization period and small-to-delay characteristics, this CDFF not only eliminates internal switching operations, but also produces less bugs at the display. The proposed flip-flop, which has a data-switching activity of 37.5 percent, will conserve up to 39 percent of the energy when operating at the same level as the quickest pulsed flip-flops. Furthermore, further timing components would be used for widespread pipelining of not only datapath portions, but also global bus interconnects, in order to maintain the pattern of better efficiency and throughput, allowing the clock system's power dissipation to become more dominant. As a consequence, lowering the electricity used by flip-flops has a significant effect on overall power use. Furthermore, although the running frequency rises, flip-flop latency occupies a significant portion of the cycle period [11]-[15]. As a result, the option and configuration of flip-flops has a significant impact on power dissipation as well as offering more slack time for better time budgeting in high-performance systems.

II. RELATED WORK

A shift register design is straightforward. An N-bit shift register is made up of N data flip-flops linked in sequence. Since there is no circuit between flip-flops in the change register, the speed of the flip-flop is less significant than the region and power usage. Due to clock propagation and skew issues, the traditional design uses more electricity. A single bit of binary data, such as 1 or 0, may be stored in a flip flop. However, numerous flip flops are needed to store multiple bits of data. Since a single flip flop may only hold one bit of information, n flip flops are attached in a certain sequence to store n bits of information. A register is a computer in digital electronics that is used to record records. In order to construct registers, flip flops are used. A register is a set of flip flops that can hold several bits of information. A collection of 16 flip flops, for example, is needed to store 16 bit data in a device. A register's input and outputs may be serial or parallel, depending on the application. Registers hold data bits in a sequence named "Byte" or "Word," where a Byte is an 8-bit array and a Word is a 16-bit collection (or 2 Bytes). A Register is an arrangement in which a number of flip flops are related in sequence. The processed data may be exchanged between the registers, which are referred to as "Change Registers." Per clock cycle, a shift register stores the data and transfers it into the performance.

III. PROPOSED WORK

The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. In digital electronics, a binary decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. They are used in a wide variety of applications, including data demultiplexing, seven segment displays, and memory address decoding. There are several types of binary decoders, but in all cases a decoder is an electronic circuit with multiple data inputs and multiple outputs that converts every unique combination of data input states into a specific combination of output states. In addition to its data inputs, some decoders also have one or more "enable" inputs. When the enable input is negated (disabled), all decoder outputs are forced to their inactive states.

A binary decoder converts binary information from n input signals to as many as 2n specific output signals, depending on its purpose. When a decoder has less than 2n output lines, at least one output pattern would be replicated for multiple input values. The integer input bits function as the "address" or bit number of the output bit that is to be

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activated in a 1-of-n binary decoder, which has n output bits. For each special mixture of input bit states, this form of decoder asserts precisely one of its n output bits, or none of them. Only when a particular, corresponding integer value is added to the inputs does and output bit become involved. If integer value 0 is added to the integer inputs, for example, output bit number 0 is chosen.

The following are some examples of this kind of decoder:

For each input value from 0 to 7, the number of numerical values that can be represented in three bits, a 3-to-8 line decoder unlocks one of eight output bits. Similarly, for each 4-bit input in the integer range 0 to 15, a 4-to-16 line decoder unlocks one of 16 outputs.

The output bits of a BCD to decimal decoder are eight. It recognizes a binary-coded decimal integer value as an input and enables one separate, unique output for each input value in the range of 0 to 9 (decimal). When a non-decimal value is added to the inputs, all outputs become disabled.

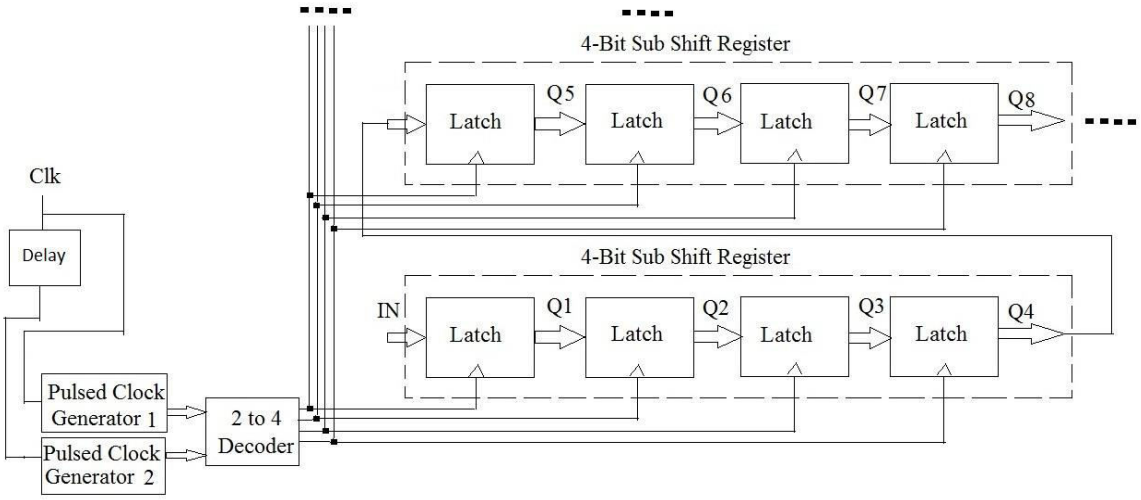

Figure.1. Proposed shift register

Figure 1 depicts an illustration of the proposed shift register. To minimize the amount of delayed pulsed clock signals, the proposed shift register is split into sub shifter registers. A 4-bit sub shifter register has five latches and uses five non-overlap delayed pulsed clock signals (CLK pulse1:4 and CLK pulseT) to execute shift operations. Four latches store 4-bit data (Q1-Q4) in the 4-bit sub shift register #1, while the last latch stores 1-bit temporary data (T1) that will be processed in the first latch (Q5) of the 4-bit sub shift register #2. The delayed pulsed clock generator generates five non-overlap delayed pulsed clock signals.

The pulsed clock signals are arranged in the same order as the five latches. The latch data T1 from Q4 is initially updated by the pulsed clock signal CLK pulse T. The pulsed clock signals CLK pulse1:4 then sequentially update the four latch details from Q4 to Q1. The latches Q2–Q4 obtain data from the latches Q1–Q3 before them, but the first latch Q1 receives data from the change register's input (IN). The other sub shift registers operate similarly to sub shift register #1, with the exception that the first latch collects data from the previous sub shift register's temporary storage latch. Because of the extra temporary storage latches, the proposed change register decreases the amount of delayed pulsed clock signals greatly, but it still raises the number of latches. Each pulsed clock signal is produced in a clock-pulse circuit consisting of a delay circuit and an AND gate, as shown in Fig. 3.12. The number of clock-pulse circuits is and the number of latches is when a shift register is split into sub shift registers. Pulsed clock signals are needed for a sub shift register with latches. Each sub shift register has a temporary storage latch, so the total number of sub shift registers is. As a result, latches for the temporary storage latches have been installed. The AND gates in the delayed pulsed clock generator in Fig. 6 can be saved by using the conventional delayed pulsed clock circuits in Fig. 4. To maintain the form of the pulsed clock in standard delayed pulsed clock circuits, the clock pulse diameter must be greater than the number of the increasing and dropping periods in both inverters in the delay circuits. Since each sharp pulsed clock signal is produced by an AND gate and two delayed signals, the clock pulsed range in the delayed pulsed clock generator in Fig. 6 may be shorter than the number of the increasing and falling periods. As a result, the delayed pulsed clock generator is well suited to the generation of fast pulsed clock signals. The number of latches and clock-

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pulse circuits varies depending on the sub shift register's word duration, which is determined by the area, power usage, and speed.

Due to the pulse skew in the cable, each pulsed clock signal arrives at the sub shift registers at a different time. The pulse skew grows in direct relation to the wire gap between the delayed pulsed clock generator and the wire. When all pulsed clock signals arrive at the same sub shift register, their pulse skews are almost identical. As a result, the pulse skew deviations between the pulsed clock signals in the same sub change register are quite tiny. The consequences of the pulse skew variations are cancelled out by the clock pulse cycles being greater than the pulse skew differences. Furthermore, since two latches linking two sub shift registers use the first and last pulsed clocks, which have a long clock pulse interval, the pulse skew variations between the various sub shift registers do not create any timing problems. Owing to parasitic capacitance and resistance, a small clock pulse cannot pass through a long wire in a long shift register. The clock pulse form is degraded at the end of the wire because the increasing and dropping periods of the clock pulse rise due to the wire delay. To retain the clock pulse form, an easy answer is to raise the clock pulse duration. However, this lowers the overall clock frequency. Inserting clock buffers and clock trees to deliver the brief clock pulse with a slight wire delay is another choice. However, this expands the field and electricity available overhead. Furthermore, multiple clock bursts result in additional overhead for multiple clock buffers and clock trees.

Because of the extra temporary storage latches, the proposed change register decreases the amount of delayed pulsed clock signals greatly, but it still raises the number of latches. Each pulsed clock signal is produced in a clock-pulse circuit consisting of a delay circuit and an AND gate, as shown in Fig. 3.12. The number of clock-pulse circuits is and the number of latches is when a shift register is split into sub shift registers. Pulsed clock signals are needed for a sub shift register with latches. Each sub shift register has a temporary storage latch, so the total number of sub shift registers is. As a result, latches for the temporary storage latches have been installed. The AND gates in the delayed pulsed clock generator in Fig. 6 can be saved by using the conventional delayed pulsed clock circuits in Fig. 4. To maintain the form of the pulsed clock in standard delayed pulsed clock circuits, the clock pulse diameter must be greater than the number of the increasing and dropping periods in both inverters in the delay circuits. Since each sharp pulsed clock signal is produced by an AND gate and two delayed signals, the clock pulsed range in the delayed pulsed clock generator in Fig. 6 may be shorter than the number of the increasing and falling periods. As a result, the delayed pulsed clock generator is well suited to the generation of fast pulsed clock signals. The number of latches and clock-pulse circuits varies depending on the sub shift register's word duration, which is determined by the area, power usage, and speed.

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IV. RESULTS AND DISCUSSION

The input and output of a serial in serial out shift register are INP and OP, respectively. The non-overlapped pulses for the first four phases are C1 to C4. To minimize the amount of delayed pulsed clock signals, the proposed shift register is split into sub shifter registers. A 4-bit sub shifter register has five latches and uses five non-overlap delayed pulsed clock signals (CLK pulse1:4 and CLK pulse T) to execute shift operations. Four latches store 4-bit data (Q1-Q4) in the 4-bit sub shift register #1, while the last latch stores 1-bit temporary data (T1) that will be processed in the first latch (Q5) of the 4-bit sub shift register #2.

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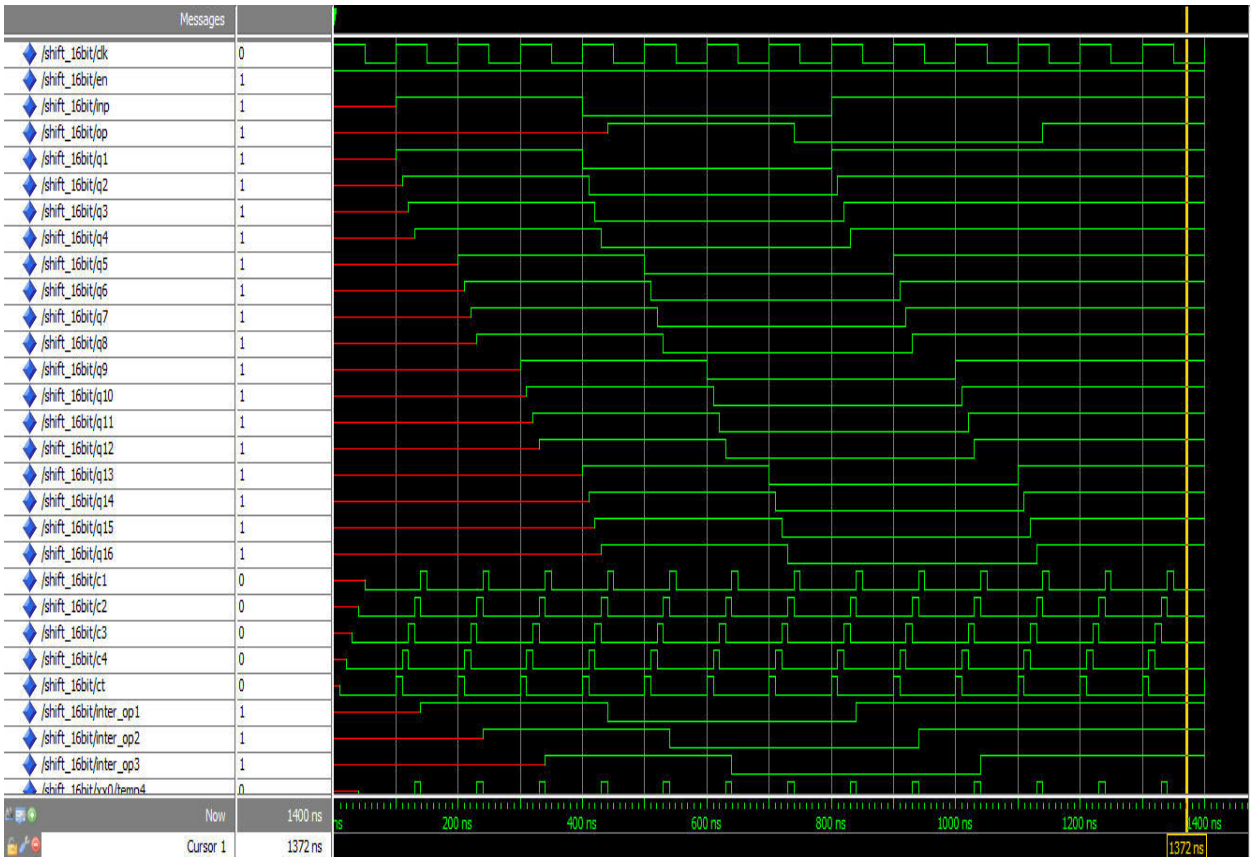

Figure.1. Simulation Results Of 16-Bit Shift Register Based On Cascaded Pulsed Generator

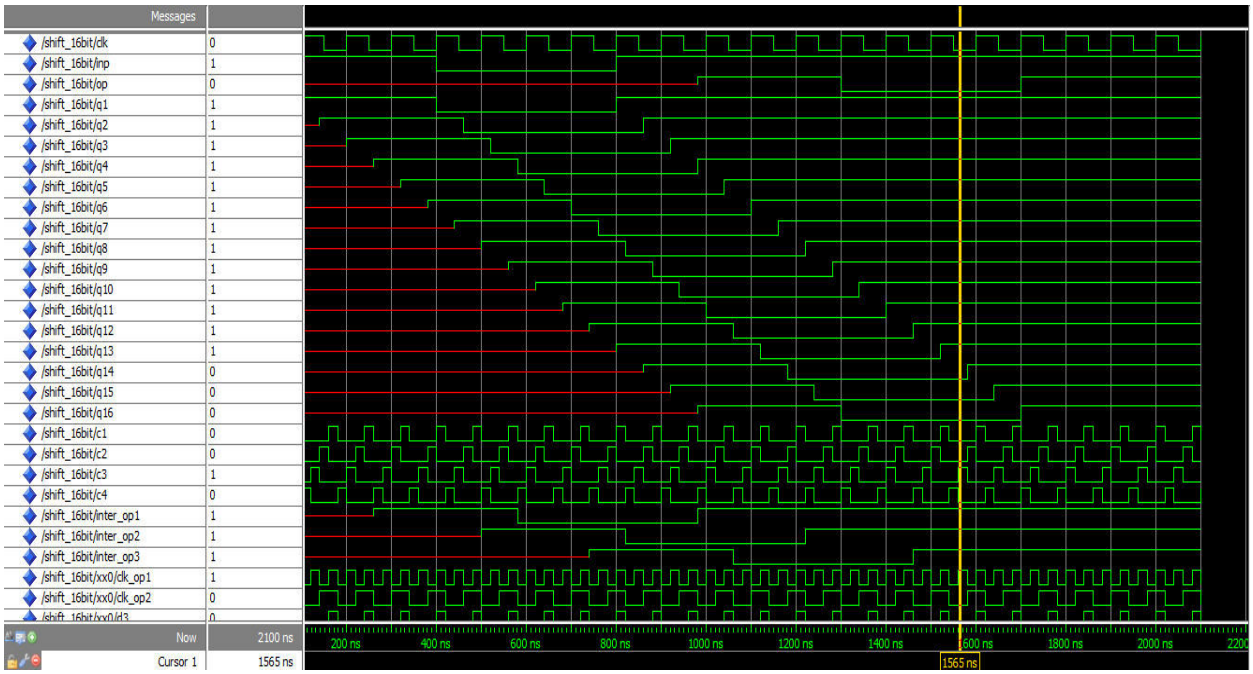

Figure.2. Simulation Results Of Proposed 16-Bit Shift Register Based On Decoder Enabled Pulsed Generator

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The input and output of a serial in serial out shift register are INP and OP, respectively. The pulses C1 to C4 are provided by a 2:4 decoder for four latches. Because of the extra temporary storage latches, the proposed change register decreases the amount of delayed pulsed clock signals greatly, but it still raises the number of latches. Since each sharp pulsed clock signal is produced from an AND gate and two delayed signals, the clock pulsed diameter can be less than the number of the increasing and falling periods. As a result, the delayed pulsed clock generator is well suited to the generation of fast pulsed clock signals.

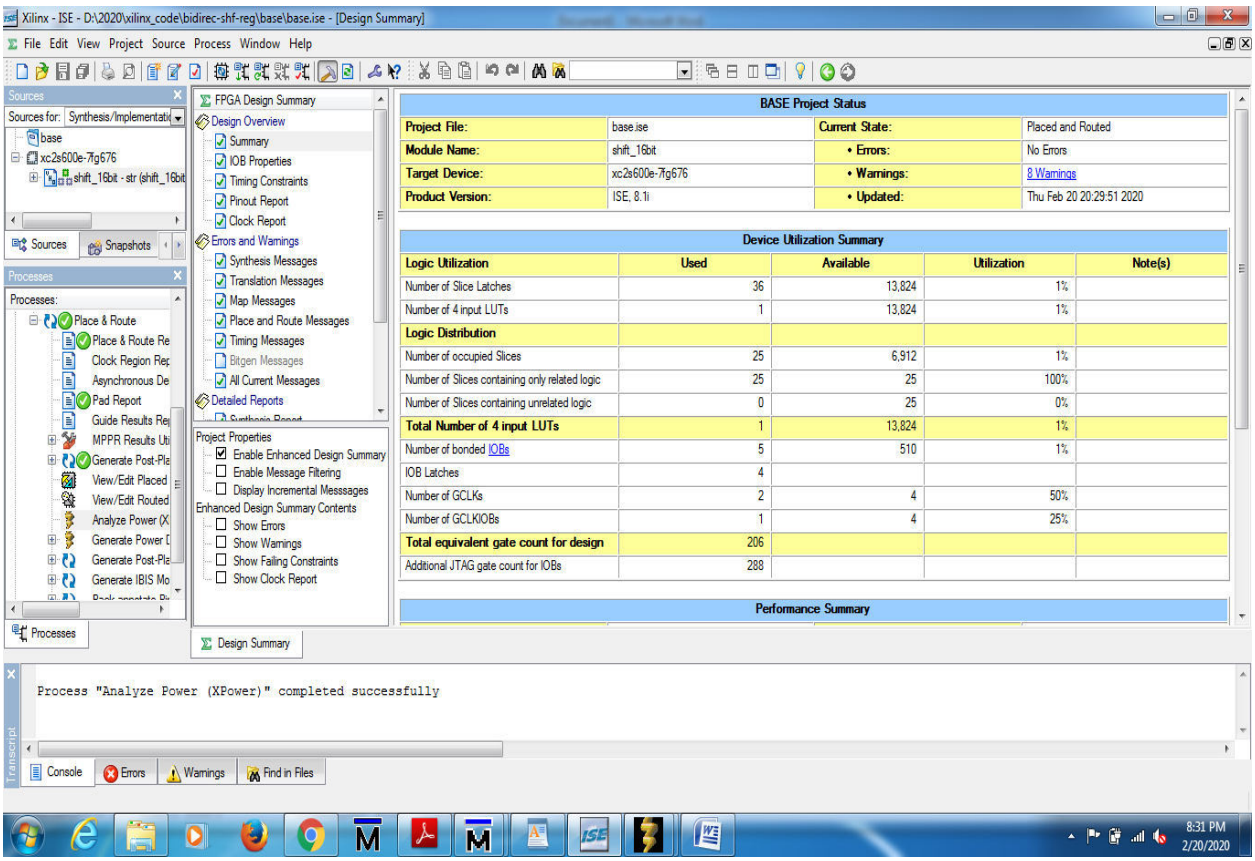

Figure.3. Area Report Of Existing 16-Bit Shift Register

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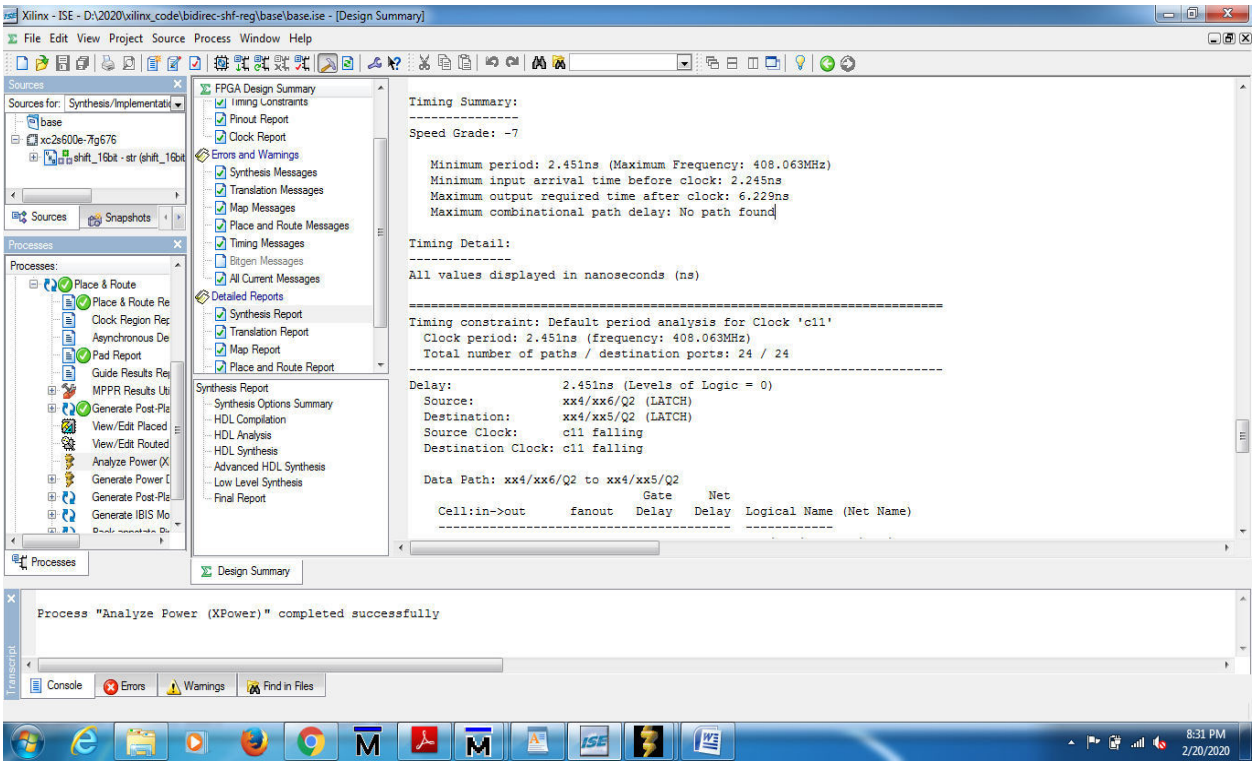

Figure.4. Delay Report of Existing 16-bit shift register

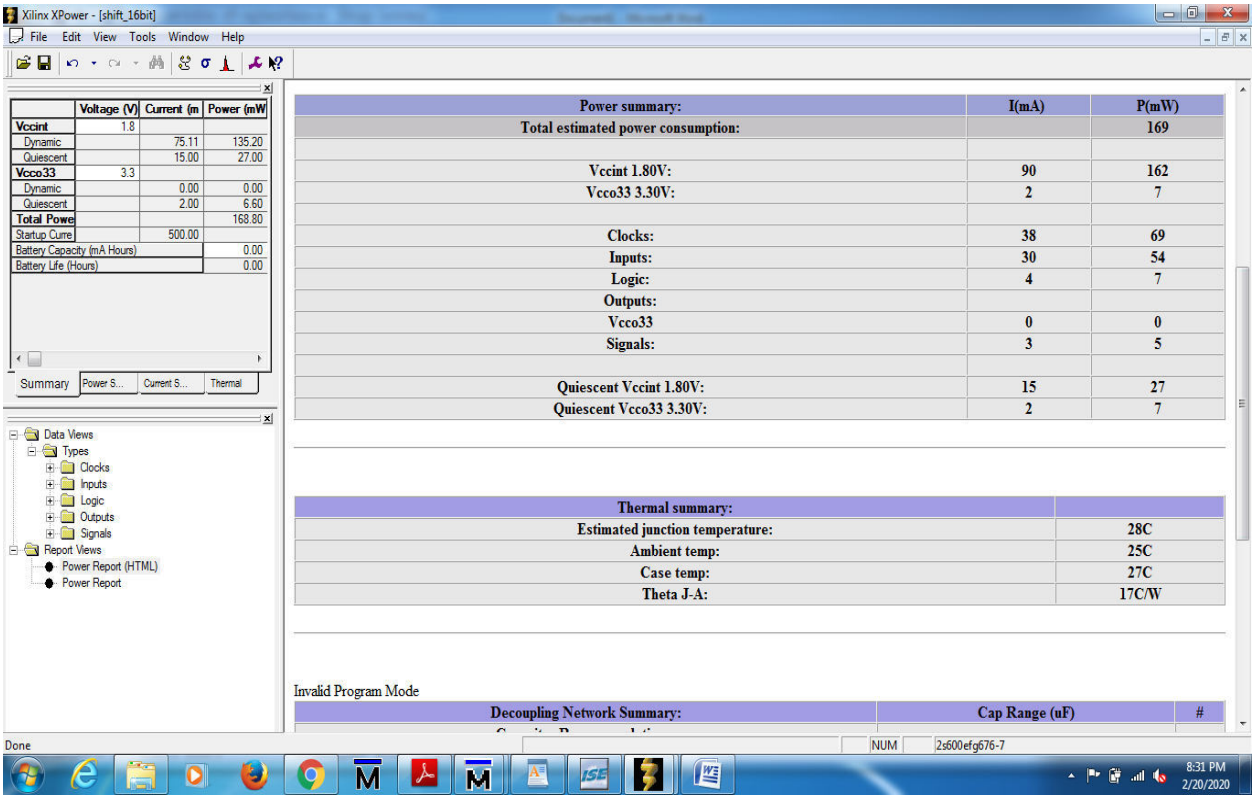

Figure.5. Power Report of Existing 16-bit shift register

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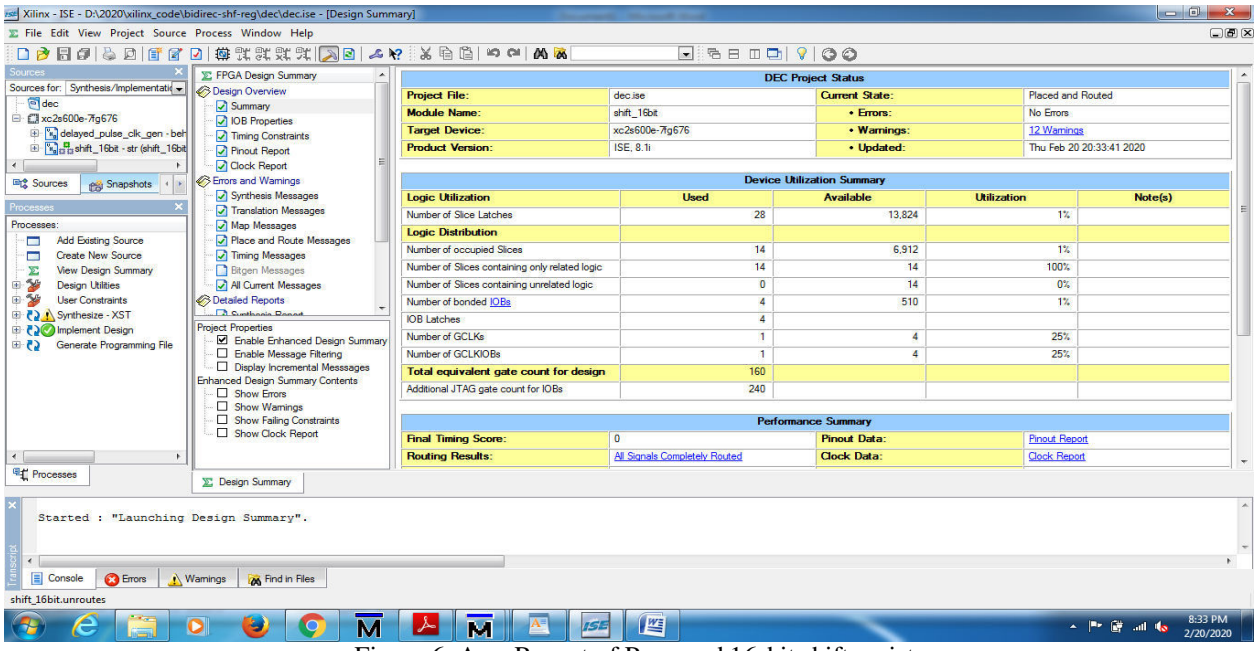

Figure.6. Area Report of Proposed 16-bit shift register

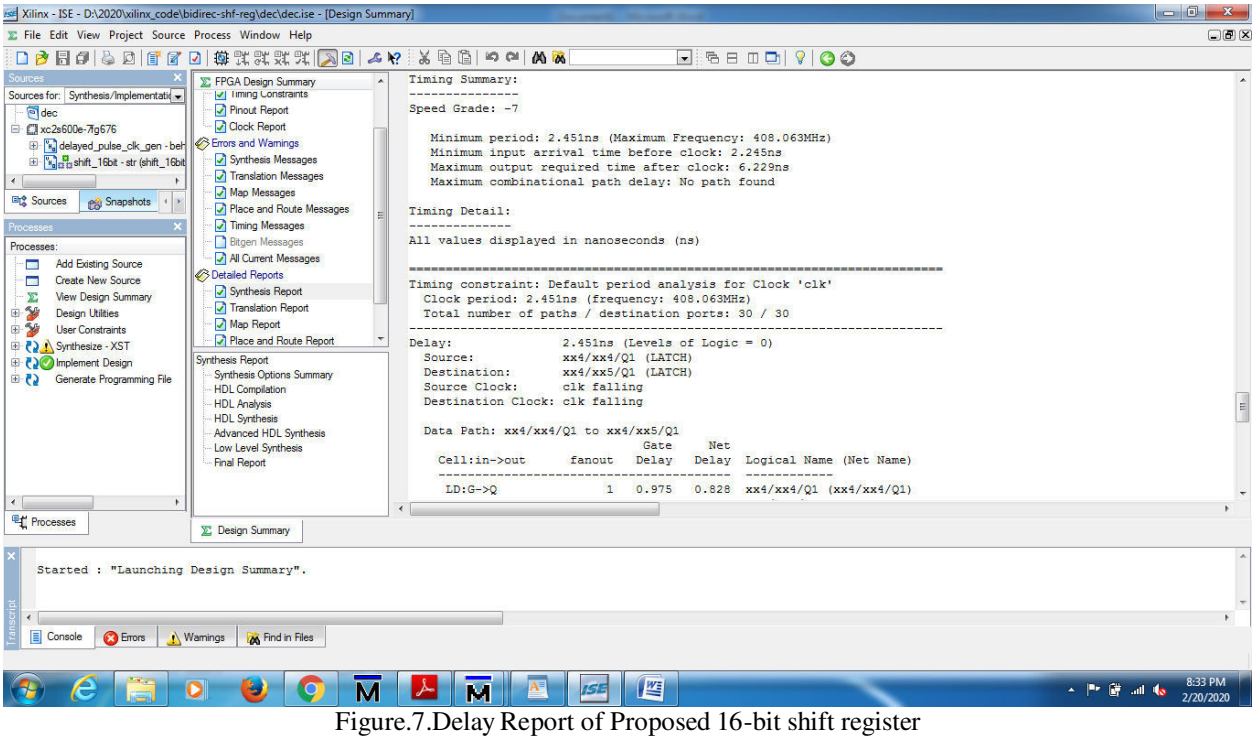

Figure.7.Delay Report of Proposed 16-bit shift register

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

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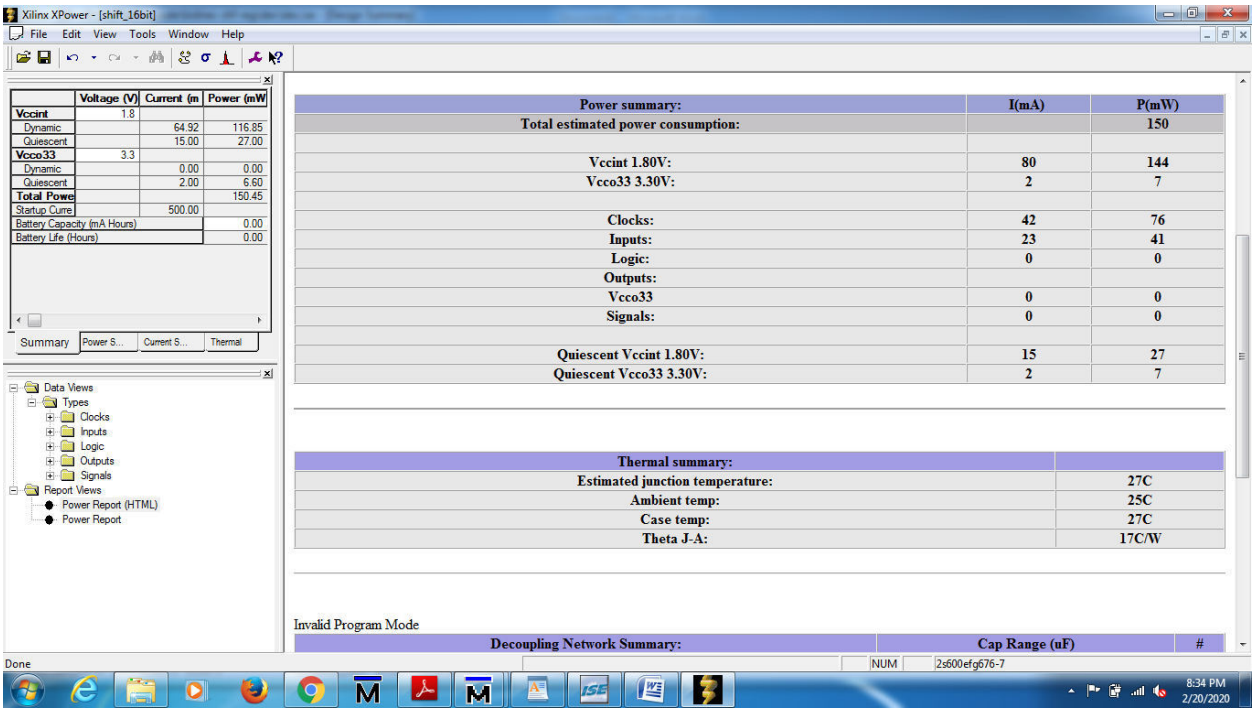

Figure.8. Power Report of Proposed 16-bit shift register

V. CONCLUSION

The use of decoder controlled pulsed latches in a low-power and area-efficient bi-directional change register is suggested. By replacing flip-flops with pulsed latches, the change register saves space and electricity. Instead of a single pulsed clock signal, the synchronization issue between pulsed latches is solved by utilizing several non-overlap delayed pulsed clock signals. By separating the latches into many sub shifter registers and utilizing extra temporary storage latches, only a limited amount of the pulsed clock signals are used. As compared to a traditional shift register with flip-flops, the proposed shift register saves 50% of the region and 19% of the electricity.

The latch-based change register proposed for SISO may also be used for SIPO, PISO, and PIPO. It may also be used in signal processing applications including Distributed arithmetic, which mostly uses a shift register to move the input samples.

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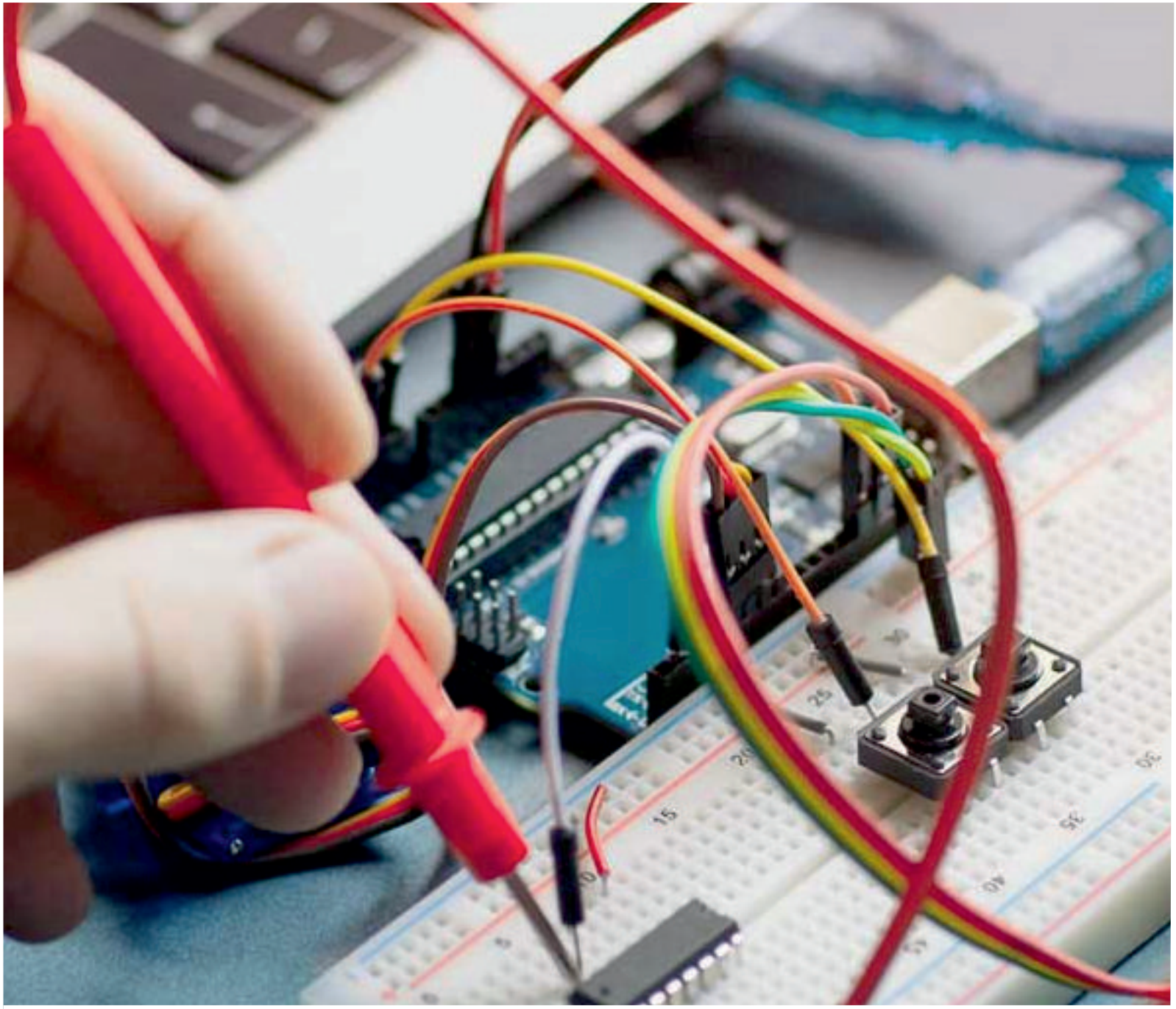

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